

Accurate Quadrature Encoder Decoding Using Programmable Logic

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Abstract— the quadrature encoder (or incremental detector) is amongst the most widely used positional feedback devices for both rotational and linear motion machines. It is well known that in conventional circuits for quadrature signals decoding, an error emerges during the direction change of the sensor movement. In some situations this error can be accumulative but in any case it provokes a position error, that is equal to the resolution (one pulse) of the sensor. A corrective algorithm is proposed here that fully eliminates this type of error. It is an improvement over a previous research of the author which is much simpler and resource saving without compromising the performance of the device. A Xilinx CPLD platform has been chosen for the experiments. The inherent parallelism of programmable logic devices permits a multi-channel CNC machine to be fully served by a single chip. This approach outperforms the capabilities of any conventional microcontroller available on the market.

Index Terms— Quadrature encoder, incremental encoder, angular position measurement, motion control, programmable logic, parallel algorithms.

I INTRODUCTION

In motion control, the quadrature encoder can be of a rotary or linear-type, with an optical or magnetic sensing principle, which gives information about both the relative position and the motional direction of a shaft. This device is directly connected to the numerical sub-system which controls the motor. Since it lies in the feedback path, it plays a very important role in keeping the system up and running. A missing pulse can lead to a major miscalculation and can even damage the mechanical drive system. The basic principle of operation is as follows: the two phases A and B of the encoder are displaced in 90 degrees each other, which allows the phase difference to be used as a sign that shows the movement direction. The time diagram of these two pulse sequences is given in fig.1.

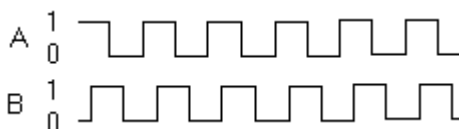


Figure 1 A time diagram of a positive direction pulse sequence

If the upper sequence determines conditionally the movement in positive direction, the pulse sequence from fig.2 visualizes the outputs A and B in the negative movement direction.

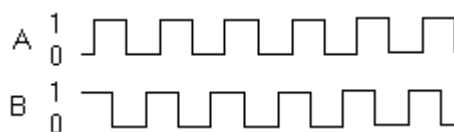


Figure 2 A time diagram of a negative direction pulse sequence

A case of direction reverse is illustrated in fig.3 by the upper two rows. In order to augment the resolution of the sensor, the frequency of pulses is being quadrupled by generating a pulse on every rising or falling edge and these higher frequency pulses are divided into two separate channels indicating positive and negative direction of movement (the lower two rows).

The transformation of the signals given in fig.3 gives opportunity for easy position measurement, using simple

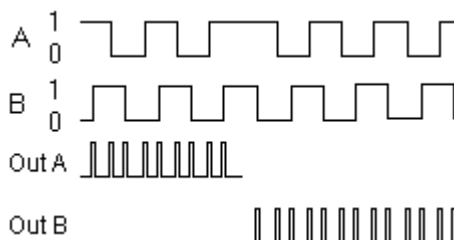


Figure 3 A case of direction change

up/down counter and easy speed measurement by using an ordinary low pass filter.

II THE ESSENCE OF THE PROBLEM

The conventional electrical circuit element commonly used to determine the direction of movement is the D-type flip-flop. The way it works is depicted in fig.4.

When Dir=1 the direction of the movement is positive and when Dir=0 - it is negative. As can be seen in the figure

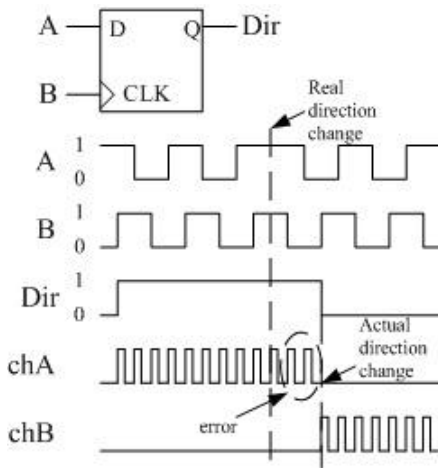


Figure 4 A conventional direction identification circuit and the emerging error

there is some delay between the actual direction change and the time of sensor activation. It is obvious from the time diagram that the two-circled pulses are on the wrong channel. If the two channels are wired to an up/down counter this will provoke an error of 2 count pulses. This is equal to the resolution of the incremental encoder, which in some cases might be of significant importance.

The general block diagram that is commonly used for the detector implementation is given in fig.5. A corrective circuit will be discussed further that updates the D-type flip-flop appropriately and fully compensates for the erroneous situations.

There exist many solutions on the market that deal with the decoding of incremental encoders. Some of them are

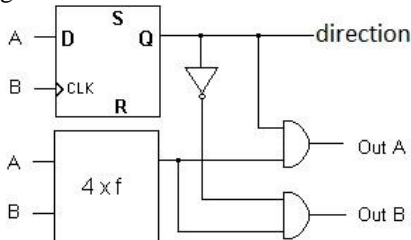


Figure 5 The conventional device block diagram

processor-based solutions [4], [8], [14], others are FPGA-based [9], [10], [12] and there exist also dedicated integrated

circuits [6], [7], to mention just a few. Although the problem is analyzed deeply and broadly discussed in the literature, none of these sources fully handles all the reversal situations and the arising errors and thus none of them fully compensates the error. Based on a previous research of the author, the aim of this work is to offer an optimized solution of the problem i.e. full elimination of the error, which is compact, resource saving and suitable for parallel implementation using programmable logic devices (PLD).

III DEFINITION OF ERRONEOUS SITUATIONS

There are 8 situations that can lead to an error during direction reversal. Four of them happen on negative clock transition (see signal B in fig.4) and they are shown in fig.6.

Another four happen on positive clock transition which is shown in fig.7.

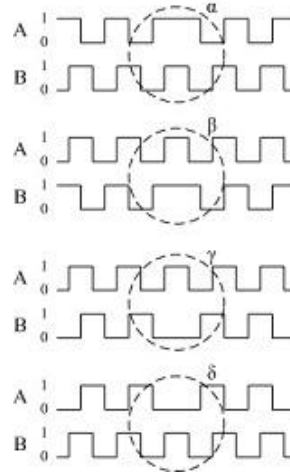


Figure 6 The reverse situations, emerging errors during the negative edge

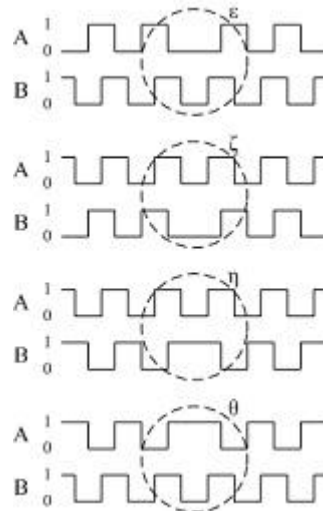


Figure 7 The reverse situations, emerging errors during the positive edge

Every one of them is assigned a letter from the Greek alphabet, namely α , β , γ , δ , ϵ , ζ , η and θ . All the situation can be described as follows:

α – the original movement is forward, the system reverses after the second positive edge. The performed transition is forward-backward.

β – the original movement is backward, the system reverses after the second positive edge. The performed transition is backward-forward.

γ – the original movement is forward, the system reverses after the first positive edge. The performed transition is forward-backward.

δ – the original movement is backward, the system reverses after the first positive edge. The performed transition is backward-forward.

ϵ – the original movement is forward, the system reverses after the second negative edge. The performed transition is forward-backward.

ζ – the original movement is backward, the system reverses after the second negative edge. The performed transition is backward-forward.

η – the original movement is forward, the system reverses after the first negative edge. The performed transition is forward-backward.

θ – the original movement is backward, the system reverses after the first negative edge. The performed transition is backward-forward.

In some situations the error emerging during direction reversal is accumulative. This is the situation when one of the ϵ or θ case combines with the other six. The probability this to happen is 0.43 and it is given in eq. 1 where P denotes the probability and C denotes the combination:

$$P = \frac{1.6 + 1.6}{C_8^2} = \frac{12}{28} = 0.4285 \cong 0.43 \quad (1)$$

IV OPERATION OF THE ERROR CORRECTION CIRCUIT

The entire device structure is implemented in Verilog HDL using the behavioral modeling approach [2], [3], [5] and represents in fact a simple finite state machine. For the sake of readability here it is presented in schematic form which is much easier to adopt. The schematic is separated in three major parts.

At first the input frequency obtained by the encoder channels A and B is being quadrupled in order to increase the sensor resolution (see fig.8). This is done using one D flip-flop per channel (a delay element) and a very simple XOR method. This way a short pulse (A_p and B_p) is produced on every rising and falling edge. Both channels are combined with an AND logic gate. At the same time a conventional direction detector algorithm works in parallel. This signal contains the error and it will be processed further.

The second stage schematic is shown in fig.9. It is comprised of one shift-register per channel which is clocked by

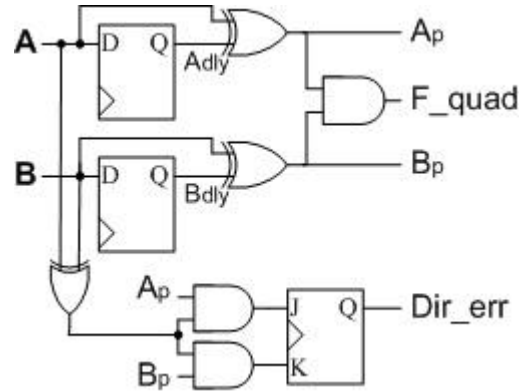


Figure 8 Frequency quadrupling and erroneous direction detector circuit

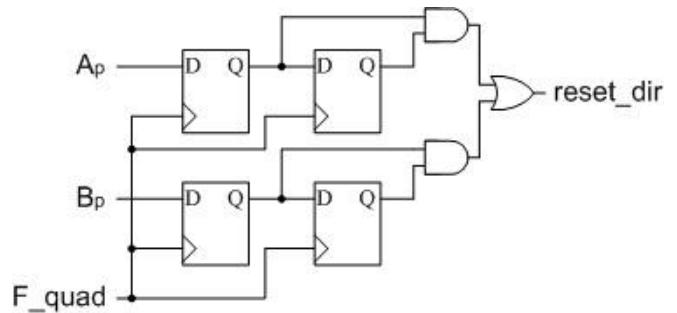


Figure 9 Direction reset circuit

the quadrupled frequency of the inputs. The AND gate permits to filter out every two consecutive pulses that may appear on the channel. The presence of such a sequence indicates the need for direction correction. The output of this circuit serves as a "reset direction" signal which emerges precisely at the time of reversal.

The "erroneous direction" and the "reset direction" signals are both used in the schematic shown in fig.10 which represents the corrective circuit. Its purpose is to set or reset the direction signal at the exact times of reversal.

Finally, the quadrupled frequency and the correct direction signals are used to drive a multiplexer circuit that out-

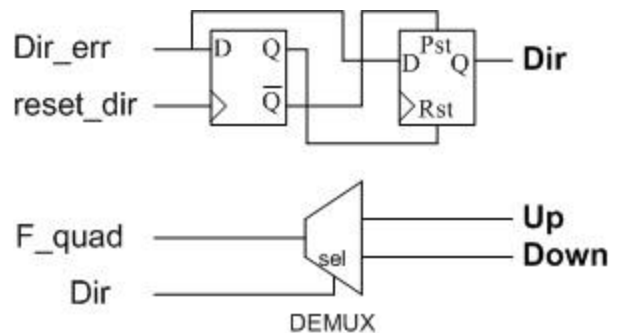


Figure 10 Corrective and output forming circuit

puts the Up and Down signals which may be used further by an up/down counter.

The entire device is built and experimented using a Xilinx CoolRunnerII CPLD programmable logic device [17].

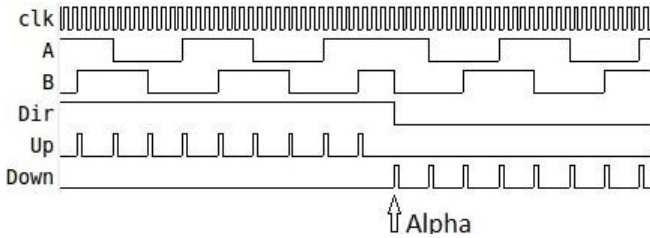


Figure 11 Case Alpha - forward-backward transition

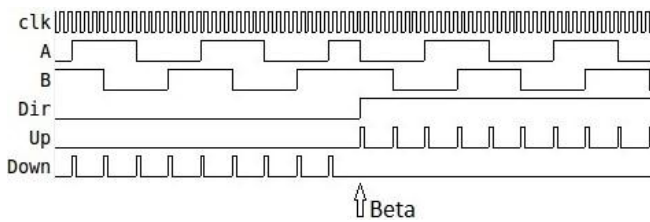


Figure 12 Case Beta - backward -forward transition

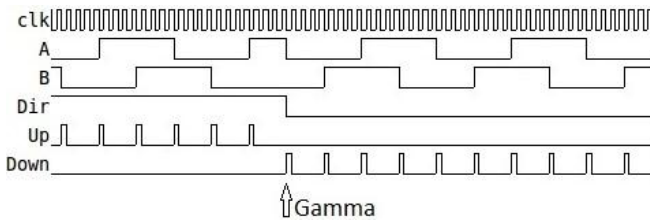


Figure 13 Case Gamma - forward-backward transition

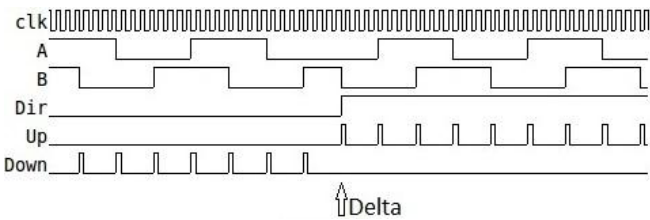


Figure 14 Case Delta - backward-forward transition

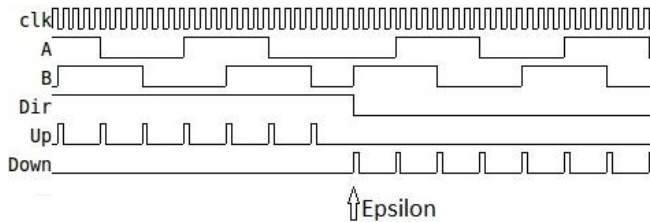


Figure 15 Case Epsilon - forward-backward transition

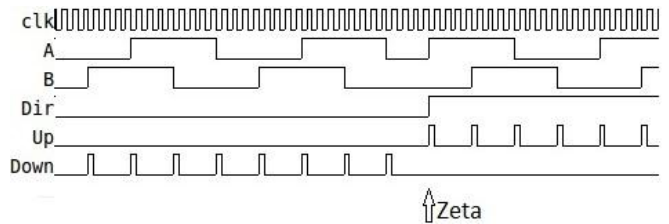


Figure 16 Case Zeta - backward-forward transition

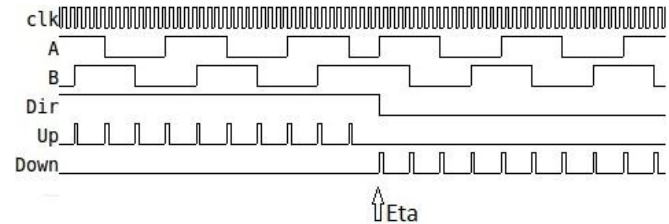


Figure 17 Case Eta - forward-backward transition

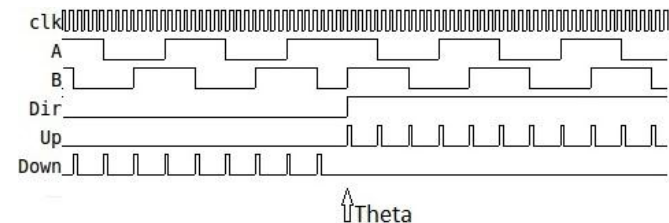


Figure 18 Case Theta - backward-forward transition

Simulation results are shown in fig.11 to fig.18, each one corresponding to a situation represented in fig.6 and fig.7 respectively.

What is not discussed here is the problem of synchronization of the inputs A and B which are asynchronous in regards to the internal clock domain of the device and thus may lead to metastability issues. These problems are very well revealed in [13], [15], [16]. A convenient digital filtering method for ignoring glitches is proposed in [9], [14].

The corrective algorithm implementation occupies 14 macrocells and 27 product terms compared with 17 macrocells and 28 product terms occupied by the design proposed in [1]. That is an improvement of 17.65 % in macrocells and permits the design to fit in a single function block, in terms of Xilinx CPLD technology. The input clock frequency is required to be at least 4 times higher than that of the quadrupled frequency while the upper limit is bounded by the resources of the chosen PLD. The abilities for parallel algorithm processing inherent to programmable logic devices gives opportunity for a multi-axis CNC machine to be fully served by a single chip.

V CONCLUSION

When it is about a high precision servo drive or motion system with a quadrature encoder-based positional feedback a fast and expensive sensor and decoding logic may be required. The proposed method suggests an error-free algorithm that handles all the erroneous situations emerging during direction reversal. The implementation of such a device is cheap and easy to be done using reconfigurable programmable logic device. Due to the capabilities for parallel algorithm execution multiple devices of the proposed type can be implemented on a single chip - be it of a CPLD or FPGA type. This approach outperforms the capabilities of any conventional microcontroller available on the market.

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